REMARKS

Claims 1, 2, 6, 10, 11, 13, 14, 16, 17, 20, 25, and 27-38 are pending. Claims 1, 10, 14, 16, and 25 have been amended and claims 3-5, 7-9, 12, 15, 18, 19, 21-24, and 26 have been canceled.

In the Office Action, claims 1, 2, 6, 9, 10, 11, 13, 16, 17, 20, 29-34, and 36-38 were rejected under 35 USC § 103(a) for being obvious in view of a Watanabe-Bean combination. Applicants request the Examiner to withdraw this rejection for the following reasons.

Claim 1 recites an extractor to extract energy from the ultracapacitor. The extractor includes a first amplifier circuit to amplify an output voltage from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor. Importantly, claim 1 recites that the first amplifier circuit is further required to "amplify the output voltage independent of a charging operation of the ultracapacitor." These features are not taught or suggested by the cited references.

The Watanabe publication discloses a charging circuit. In fact, its entire disclosure is dedicated to charging a capacitor. Thus, while the Watanabe publication discloses an amplifier circuit, it does not teach or suggest an amplifier circuit that operates "independent of a charging operation" of its capacitor. On the contrary, Watanabe expressly teaches away from the features recited in claim 1.

To make these differences even more apparent, claim 1 has been amended to recite that the first amplifier circuit amplifies the output voltage "during a time when the load is to be driven by the amplified output voltage." Watanabe does not teach or suggest these features.

Moreover, claim 1 recites "a controller to generate a second control signal to vary a ratio of the divider, the varied ratio adjusting the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage of the load." The Watanabe publication discloses a voltage divider circuit formed from two resistors 9 and 10. (See Figs. 1, 7, and 19). At Paragraph [0102], Watanabe further discloses setting the division ratio of these resistors, and how the resistance of each resistor is computed. However, Watanabe does not teach or suggest a control circuit that varies the ratio of its voltage divider in order to maintain an output voltage equal to or above a voltage of a load.

The Bean publication discloses an ultracapacitor. However, Bean does not teach or suggest the features of claim 1 missing from Watanabe.

Based on these differences, it is respectfully submitted that claim 1 and its dependent claims are allowable over a Watanabe-Bean combination.

Claim 10 recites that "the adiabatic amplifier is to amplify the voltage output from the ultracapacitor independent of a charging operation of the ultracapacitor and during a time when the load is to be driven by the amplified output voltage." These features are not taught or suggested by the Watanabe and Bean publications, whether taken alone or in combination.

Also, claim 10 recites first and second transmission gates that are alternatively switched to "output an amplified differential signal that corresponds to the amplified voltage of the ultracapacitor." The Watanabe publication does not disclose these features, i.e., Watanabe discloses switches 4A-4D. However, these switches do not switch an **amplified** voltage. Rather,

because the switches are coupled to the input side of the transformer which performs the amplification function, it is clear that switches 4A-4D do not switch an "amplified" voltage. Rather, these switches switch a voltage from DC power source 1 in its unamplified state.

Moreover, as those skilled in the art very clearly understand, switches 4A-4D form an inverter circuit does not in any way perform the function of amplifying a voltage. Rather, the inverter circuit is switches for the sole purpose of changing a DC voltage signal into an AC voltage signal.

The Bean patent fails to teach or suggest the features of claim 10 missing from the Watanabe publication.

Based on these differences, it is respectfully submitted that claim 10 and its dependent claims are allowable over a Watanabe-Bean combination.

Claim 11 recites the additional features of a "controller to monitor a change in the amplified voltage" and "a voltage regulator to adjust the amplified differential signal to cause the amplified voltage of the ultracapacitor to be substantially equal to or above the first predetermined voltage." In the Office Action, the Examiner compared the controller to inverter controller 13. However, this controller is only used to switch the inverter circuit formed from switches 4A-4D.

As those skilled in the art very clearly understand, the inverter circuit of Watanabe does not in any way perform the function of monitoring a change in any type of voltage, let alone an amplified voltage. Rather, the inverter circuit is controlled by controller 13 to change a DC

voltage signal into an AC voltage signal. That is why the switch of 4A-4D is performed in the first place. Applicants submit that claim 11 is allowable based on these additional differences.

Claim 14 recites features similar to those which patentably distinguish claim 1 from a Watanabe-Bean combination. Applicants therefore submit that claim 14 and its dependent claims are allowable.

Claim 16 recites that the varied ratio in claim 14 "adjusts the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage during a time when the detected voltage of the ultracapacitor is above a second predetermined voltage of an amplifier circuit that is to perform said amplifying." These features are not taught or suggested by Watanabe, whether taken alone or in combination with Bean.

As shown in Fig. 11, the Watanabe publication discloses a divider circuit formed from resistors 9 and 10. Watanabe also discloses, at Paragraph [0102], setting the division ratio of these resistors, and how the resistance of each resistor is computed. However, Watanabe does not teach or suggest in Paragraph [0102] or in any other paragraph adjusting a first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage during a time when the detected voltage of the ultracapacitor is above a second predetermined voltage of an amplifier circuit that is to perform said amplifying.

Applicants therefore submit that claim 16 is allowable, not only by virtue of its dependency from claim 14 but also based on the features separately recited therein.

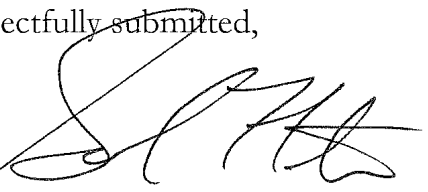
Claim 25 recites features similar to those which patentably distinguish claim 1 from a Watanabe-Bean combination. Applicants therefore submit that claim 25 and its dependent claims are allowable.

Claims 27, 28, and 35 were rejected under 35 USC § 103(a) for being obvious in view of a Watanabe-Bean-Sasaki combination. This rejection is traversed on grounds that the Sasaki patent does not teach or suggest the features of base claims 1 and 25.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and timely allowance of the application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,



Attorney for Intel Corporation

Samuel W. Ntiros
Registration No. 39,318

P.O. Box 221200
Chantilly, Virginia 20153-1200
703 766-3701 DYK/SWN:knh